HEI 9-83920

[0011]

[Means for Solving the Problems]

The invention described in claim 1 is provided with a detecting means for detecting whether a protection signal to protect the copy right is superimposed to an input video signal or not and an inhibiting means to inhibit output of the video signal based on detection of the detecting means.

[0012]

[Operation]

According to the present invention, when the detecting means detects the protection signal from the input video signal, the inhibiting means inhibits output of the video signal to a printer, etc.

[0013]

[Preferred Embodiment of the Invention]

Fig. 1 shows an embodiment of the present invention and the elements which are substantially same as those in Fig. 6 are designated by the same reference numerals and the same description is not repeated here. Content explained below is only an embodiment of a video processing apparatus comprising a means for discretely diversifying a video signal, a means for temporarily storing such discrete values and a means for processing the discrete values stored temporarily and printing the image on a sheet. This video processing apparatus can be applied to all video processing apparatus providing the means explained above. Structure of Fig. 1 is

different from Fig. 6 in that a copy guard detecting means 220 is provided in a synchronous isolating means 202. This copy guard detecting means 220 transmits the detecting signal of "L" level (low level) to a video processing means 207 when it is detected that the copy guard signal is superimposed, as the protection signal to protect the copy right, to the video signal input from a signal generator 1 such as VTR, etc. via an input means 201.

[0014]

Fig. 2 is a block diagram illustrating a first embodiment of the video processing means 207 shown in Fig. 1. In Fig. 2, the circuits other than the A/D converting means 204, memory 205, memory 206 and recording means 208 are included within the video processing means 207.

[0015]

2001 designates a ROM storing the predetermined video data such as characters and this video data is arranged in the same address area as the memory 205. 2003 designates an AND gate for obtaining negative logic between a write acknowledgment signal WE from the video processing control means 2002 and a detecting signal P obtained from a copy guard detecting means 220 and an output of this AND gate is input to the ROM 2001 as a data output acknowledgment signal OE. Like the memory 205 storing the video data, the ROM 2001 is given the address I from the video processing control means 2002.

[0016]

2002 designates the video processing control means for controlling the video processing to be executed in the video processing means 207, while 2006 designates a gate means to obtain a logical AND between the video data DAD sent from the A/D converting means 204 and data ROD from ROM 2001. 2007 designates a selector which is switched to store the output data DG of gate means 2006 to the memory 205 when the write acknowledgment signal WE from the video processing control means 2002 is in the L level. The memory 205 is controlled by the signals WE, OE from the video processing control means 2002. Moreover, the memory 206 is also assumed to be controlled by the status of the video processing control means 2002. 2008 designates a data bus on which the data of the memory 205, memory 206, recording means 208 and video processing control means 2002 is transmitted.

[0017]

Next, operation of each portion of Fig. 2 will be explained with reference to Fig. 3. In the step 1 of Fig. 3, the copy guard detecting signal P becomes L level when the copy guard detecting means 220 detects the copy guard signal from the input video signal. In the step 2, the video data DAD from the A/D converting means 204 is output with the clock signal from the PLL means 203. Simultaneously, the address I is output from the video processing control means 2002. In the step 3, when the write acknowledgment signal WE becomes L level, an output of the AND gate 2003 becomes L level because it is ANDed with the copy guard detecting

signal P. Therefore, the output acknowledgment signal OE of ROM 2001 becomes L level and the data ROD of the ROM 2001 is output.

[0018]

In the step 4, the video data ROM and DAD are ANDed by the gate means 2006 and thereby the data GD is output. The selector 2007 makes the selecting operation so that the data GD is given to the memory 205 by the signal WE. This data is stored, as the data RMD, to the memory 205 by the signal WE in the L level. In the step 5, since the address I and signal WE are negated, an output of the AND gate 2003 is also negated. Accordingly, the data ROD of the ROM means 2002 is invalidated. Moreover, in regard to the output of selector 2007, the output data RMD from the memory 205 is sent to the bus 2008 because the signal WE is negated. As the data DAD from the A/D converting means 204, the next pixel data is output by the system clock from the PLL means 203.

[0019]

According to the above operations, when the copy guard detecting signal P is L level, namely when the copy guard signal is superimposed to the video signal, the video data DAD from the A/D converting means 204 is masked by the data ROD from the ROM2001. Accordingly, as the result of this embodiment, when the data stored in the ROM2001 is given to form, for example, the characters "invalid" and such video data is recorded by the recording means 208, the characters "invalid" are written as the image on the sheet and thereby

original image cannot be reproduced. Moreover, since the characters "invalid" are also displayed on the screen of a monitor 3, warning for copy right protection can be issued to a printer user. In addition, the characters "invalid" may be replaced with mosaic image. Namely, it is enough when the data can distort the original image.

[0020]

Fig. 4 is a block diagram for explaining the second embodiment. The portions like those of Fig. 2 are not explained here. In Fig. 4, 2010 designates a counter which may be replaced with the ROM2001 of Fig. 2 and is synchronously driven by the system clock not illustrated. The count acknowledgment/EN signal is an output of the AND gate 2003. Moreover, a ripple carry signal RP of this counter 2010 is input to the gate means 2006 via the AND gate 2009 of negative logic. When the number of bits of counter 2001 is assumed as W and width of the address I generated from the video processing control means 2002 is assumed as V, the relationship $W \ll V$ can be obtained and such value is set to allow a plurality of mask pixels to appear on the image obtained from the A/D converting means 204. One input of the AND gate 2009 is an output of the AND gate 2003.

[0021]

Operation of each portion of Fig. 4 will be explained with reference to Fig. 5. In the step 1, when the copy guard detecting means 220 detects the copy guard signal, the copy guard detecting signal P becomes L level. In the step 2, the

clock signal from the PLL means 203 causes the A/D converting means 204 to output the video data DAD. Simultaneously, an address I is output from the video processing control means 2002. In the step 3, since the signal WE becomes L level, an output of the AND gate 2003 becomes L level as a result of logical AND with the copy guard detecting signal P. Therefore, the signal EN of the counter 2010 becomes L level and counting-up is executed synchronously with the rising edge of the system clock not illustrated (Fig. 5 shows particularly a profile when the ripple carry signal RP is generated).

[0022]

In the step 4, the signal RP becomes L level. The gate means 2006 obtains logical AND of the video data DAD and signal RP and thereby the data GD becomes L level totally. The selector 2007 is switched with the signal WE to give the data GD to the memory 205. This data is stored, as the data RMD, to the memory 205 with the signal W of the L level. In the step 5, when the address I, signal WE are negated, an output of the AND gate 2003 is negated and an output of the AND gate 20009 is also negated making the signal RP invalid and the data GD becomes similar to the video data DAD. Moreover, in regard to an output of the selector 2007, when the signal WE is negated, an output data RMD from the memory 205 is transmitted to the bus 2008. As the data DAD from the A/D converting means 204, the next pixel data is output by the system clock from the PLL means 203.

[0023]

According to above operations, when the copy guard detecting signal P is level, namely when the copy guard signal is superimposed to the video signal, the video data DAD from the A/D converting means 204 is masked by the signal RP from the counter 2010. The video data stored in the memory 205 includes noise through the setting that the masking position of /RP of the counter 2010 is not interpolated with the video signal. Therefore, as a result of the second embodiment, when the video data is recorded by the recording means 208, noise is included in the image on the sheet and thereby the original image cannot be reproduced. Moreover, since noise of the signal RP of the counter 2010 is displayed on the display screen of the monitor 3, the warning for copy right protection can be issued to a printer user.

[0024]

[Effect of the Invention]

As explained above, according to the present invention, if it is attempted to record an image of the video signal to which the copy guard signal is superimposed on a sheet using a printer, such image is never recorded and the original image cannot be reproduced in order to protect the copy right and moreover an image is never displayed on the screen of monitor. Thereby, the warning for copy right can be issued to a user.

Fig. 1:

1: Signal generator; 2: Video processing apparatus;

201: Input means; 202: Synchronous isolating means;

203: PLL means; 204: A/D converting means;

205: Memory; 206: Memory; 207: Video processing means;

208: Recording means; 209: D/A converting means;

210: Synchronous signal adding means;

212: Output means; 213: Control means;

215: Operating means;

Fig. 2:

204: A/D converting means; 205: Memory; 206: Memory;

208: Recording means;

2002: Video processing control means; Address WE;

2006: Gate means; 2008: Bus;

Fig. 3:

Step; ROM 2001;

Fig. 4:

204: A/D converting means; 205: Memory; 206: Memory;

208: Recording means; 2010: Counter; Carry;

2006: Gate means; 2008: Bus;

2002: Video processing control means; Address;

Fig. 5:

Step; Counter 2010;

Fig. 1
【図１】

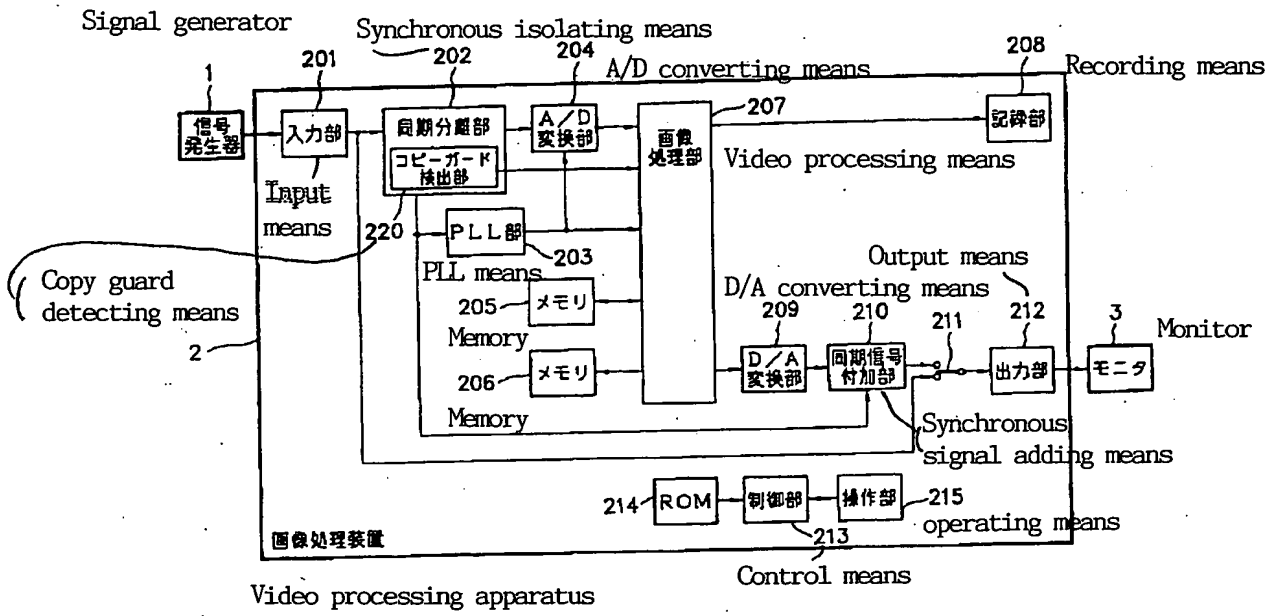

Fig. 2
【図２】

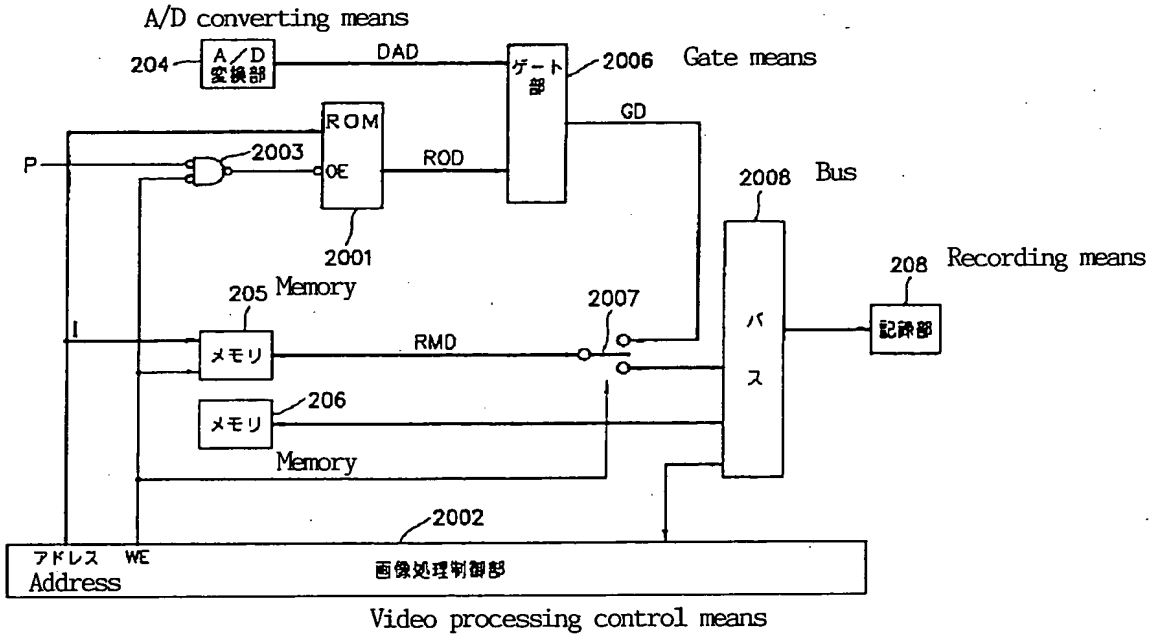

Fig. 3
【図３】

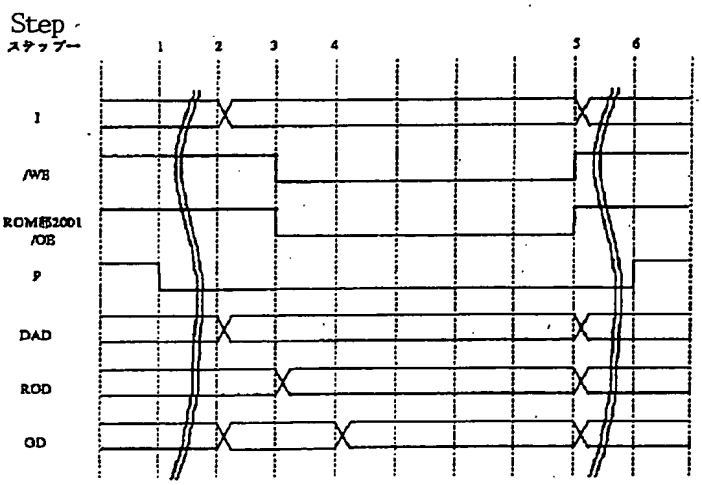

Fig. 4
【図４】

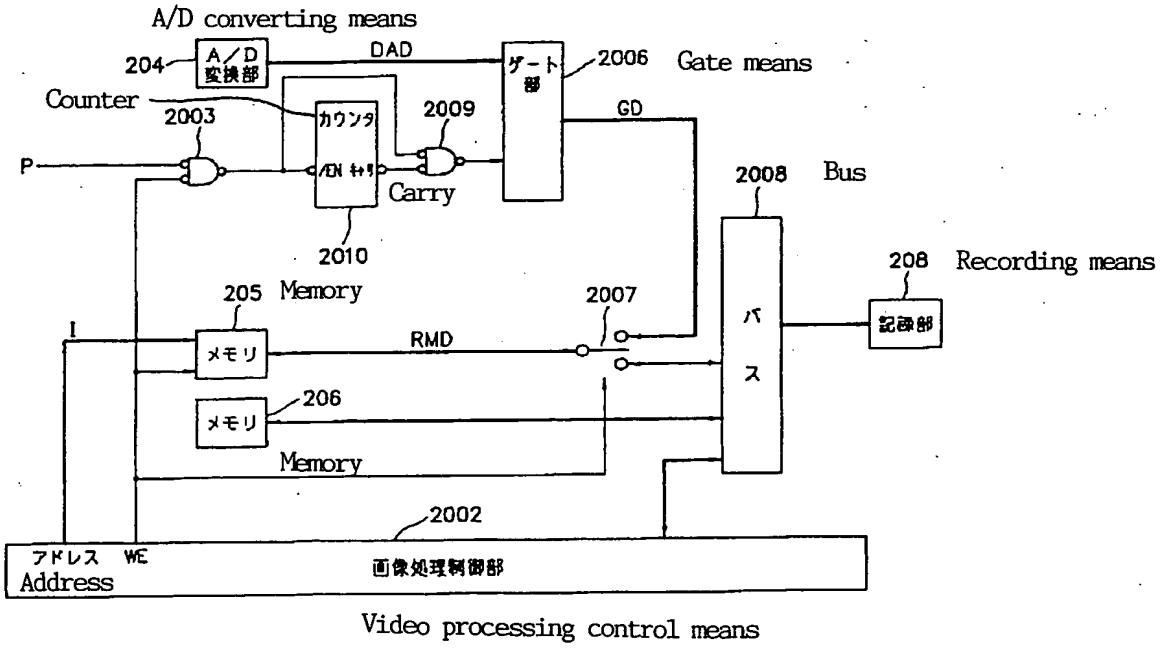

Fig. 5
【図５】

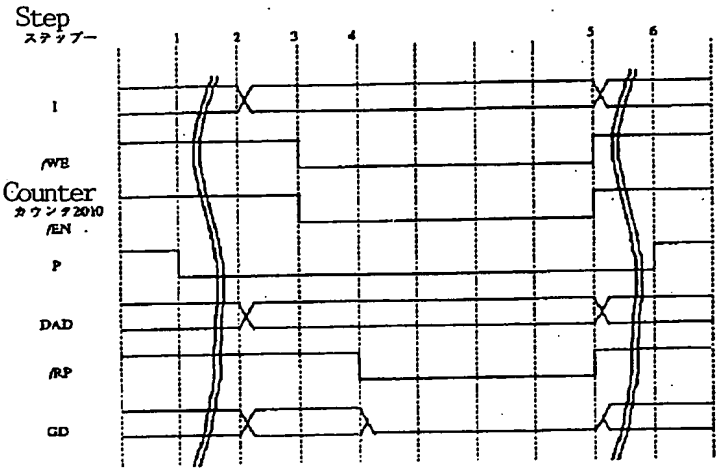

Fig. 6
【図６】